

WHAT IS CLAIMED IS:

*SBWY* 1. A method of manufacturing an LDMOS transistor comprising:

5 providing a semiconductor substrate of a first conductivity type having a well region of a second conductivity type formed on a surface thereof;

10 implanting ions of the first conductivity type into a part of the well region with a predetermined energy;

15 subjecting the substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the substrate;

20 forming a gate oxide layer and a gate electrode on the surface of the substrate; and

25 forming a drain region on the surface of the substrate, wherein the predetermined energy is set so that an accelerated oxidation during a formation of the gate oxide layer is inhibited.

2. A method of manufacturing an LDMOS transistor

according to claim 1, wherein said implantation is conducted as a high energy ion implantation.

*SBWY* 3. A method of manufacturing an LDMOS transistor according to claim 1, wherein the predetermined energy is about 500KeV.

25 4. A method of manufacturing an LDMOS transistor according to claim 1, wherein said implantation is conducted with a dosage of about  $5.0 \times 10^{15}/\text{cm}^2$ .

*Sub 46* > 5. A method of manufacturing an LDMOS transistor according to claim 1, wherein said implantation is conducted into a region of the substrate where the drain region is formed.

6. A method of manufacturing an LDMOS transistor  
5 according to claim 1, wherein the drain region is a reduced surface drain.

*Scope* > 7. A method of manufacturing an LDMOS transistor comprising:

10 providing a semiconductor substrate of a first conductivity type having a first well region of a second conductivity type formed on a surface thereof, and a second well region of the first conductivity type formed within the first well;

15 implanting ions of the second conductivity type into a part of the second well region with a predetermined energy;

subjecting the substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the second conductivity type on the surface of the substrate within the second well;

20 forming a gate oxide layer and a gate electrode on the surface of the substrate; and

25 forming a drain region on the surface of the substrate, wherein the predetermined energy is set so that an accelerated oxidation during a formation of the gate oxide layer is inhibited.

8. A method of manufacturing an LDMOS transistor according to claim 7, wherein said implantation is conducted

as a high energy ion implantation.

~~Step 8~~ 9. A method of manufacturing an LDMOS transistor according to claim 7, wherein the predetermined energy is about 500KeV.

5 10. A method of manufacturing an LDMOS transistor according to claim 7, wherein said implantation is conducted with a dosage of about  $5.0 \times 10^{15}/\text{cm}^2$ .

~~Step 9~~ 11. A method of manufacturing an LDMOS transistor according to claim 7, wherein said implantation is conducted into a region the substrate where the drain region is formed.

10 12. A method of manufacturing an LDMOS transistor according to claim 7, wherein the drain region is a reduced surface drain.

~~Step 10~~ 13. A method of manufacturing an LDMOS transistor comprising:

15 providing a semiconductor substrate of a first conductivity type having a first well of a second conductivity type formed on a surface thereof within a first region, and a second well of the first conductivity type formed within a second region that is inside of the first region;

20 implanting ions of the second conductivity type into the second well with a predetermined energy;

25 subjecting the substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the second conductivity type located in a third region that is inside of the second region;

forming a gate oxide layer and a gate electrode on the surface of the substrate, the gate oxide layer extending from the first region to the third region through the second region; and

5 ~~14~~ forming a drain region on the surface of the substrate within the first region, wherein the predetermined energy is set so that an accelerated oxidation during a formation of the gate oxide layer is inhibited.

10 14. A method of manufacturing an LDMOS transistor according to claim 13, wherein said implantation is conducted as a high energy ion implantation.

15 ~~15~~ 15. A method of manufacturing an LDMOS transistor according to claim 13, wherein the predetermined energy is about 500KeV.

16. A method of manufacturing an LDMOS transistor according to claim 13, wherein said implantation is conducted with a dosage of about  $5.0 \times 10^{15}/\text{cm}^2$ .

20 ~~16~~ 17. A method of manufacturing an LDMOS transistor according to claim 13, wherein said implantation is conducted into a region the substrate where the drain region is formed.

18. A method of manufacturing an LDMOS transistor according to claim 13, wherein the drain region is a reduced surface drain.